

Fig. 1

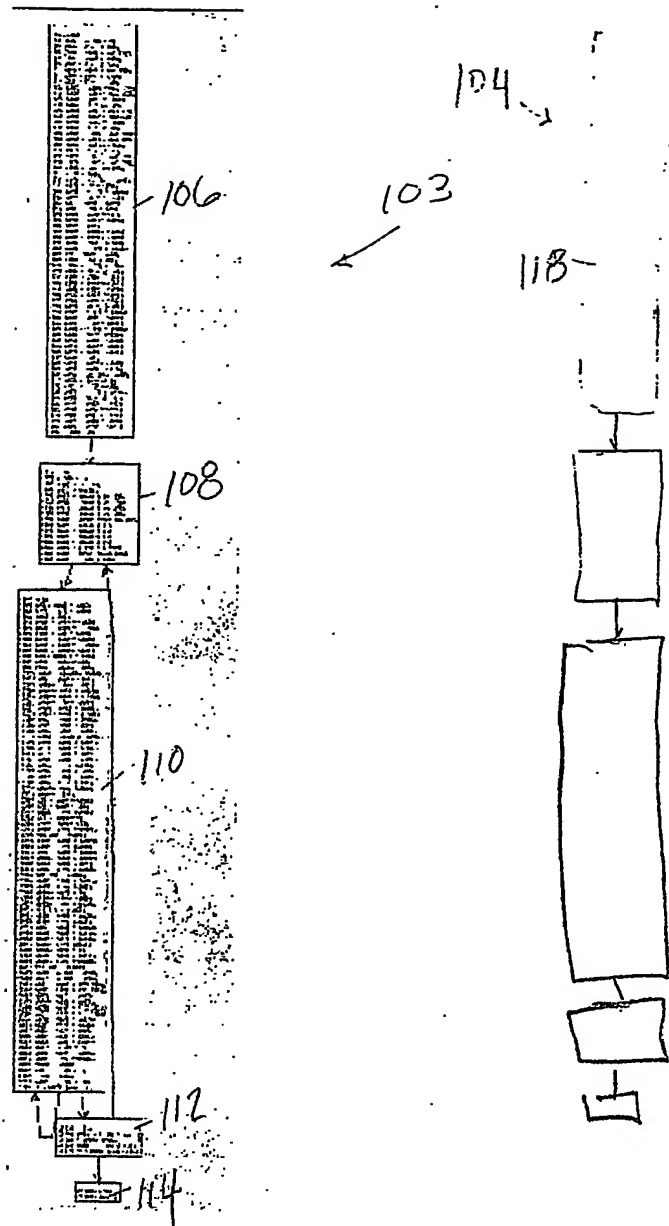


Fig. 2

(1) 125 =  
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106

Fig. 3

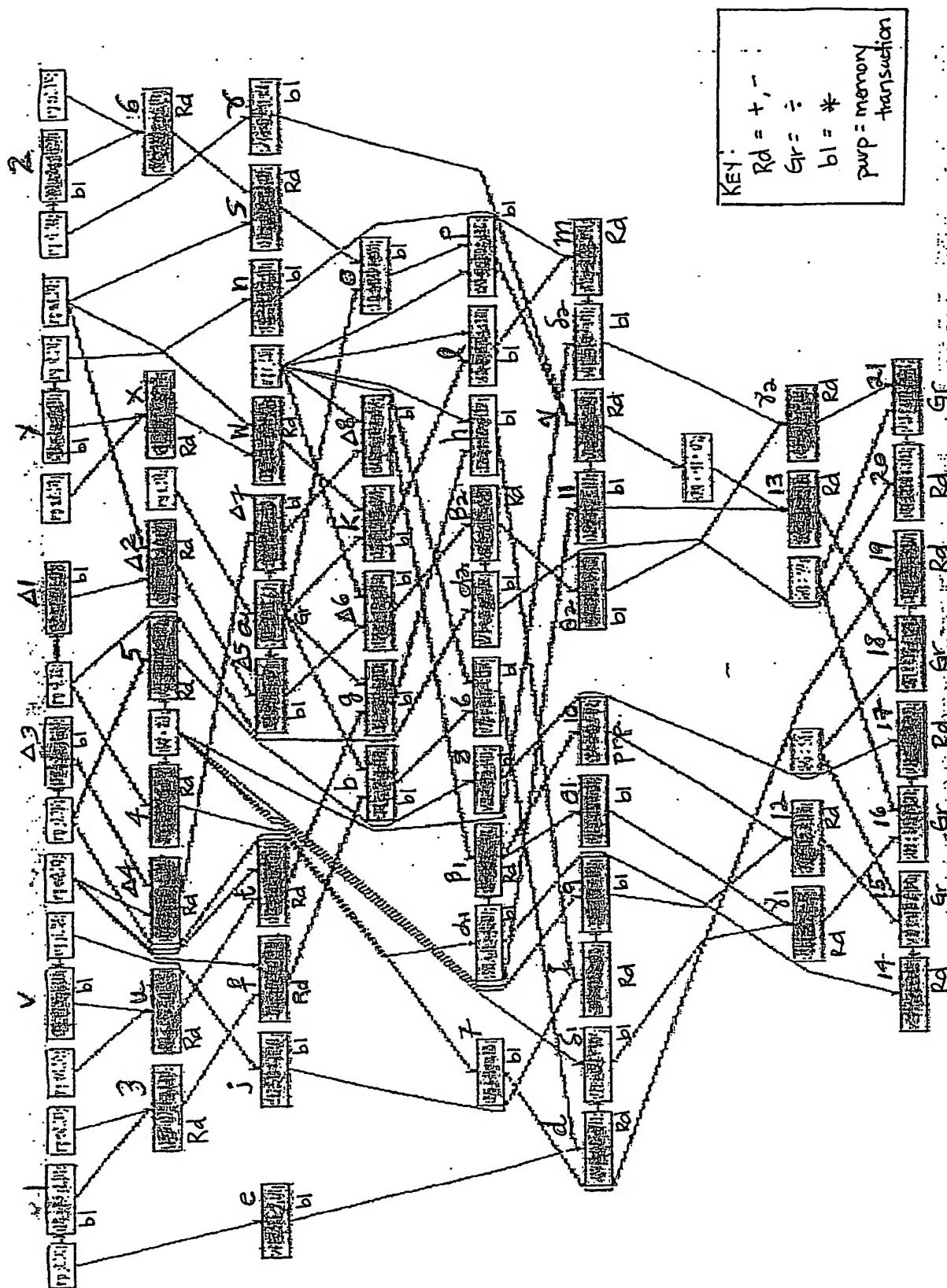


Fig. 4(a)

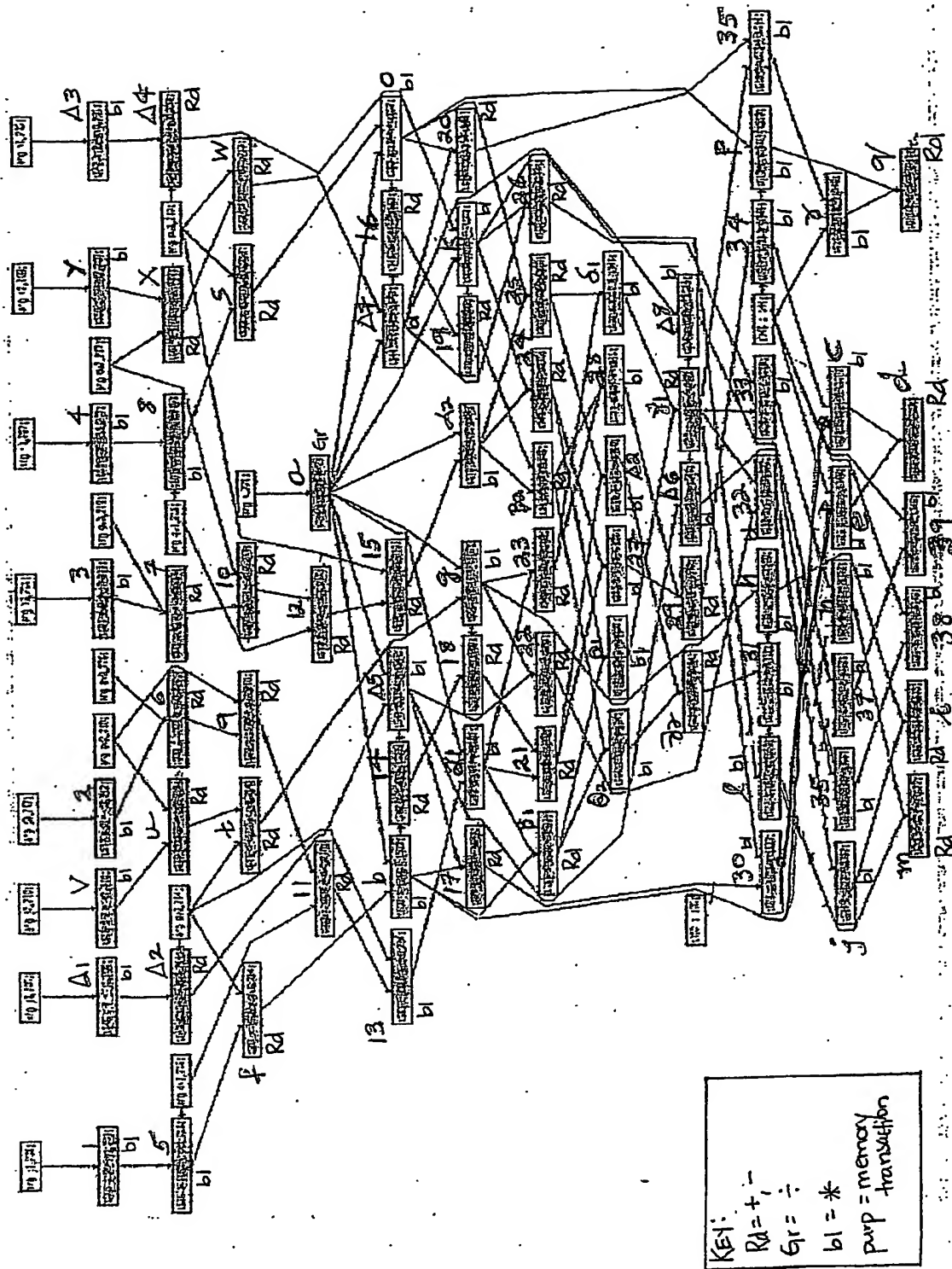


Fig. 4(b)

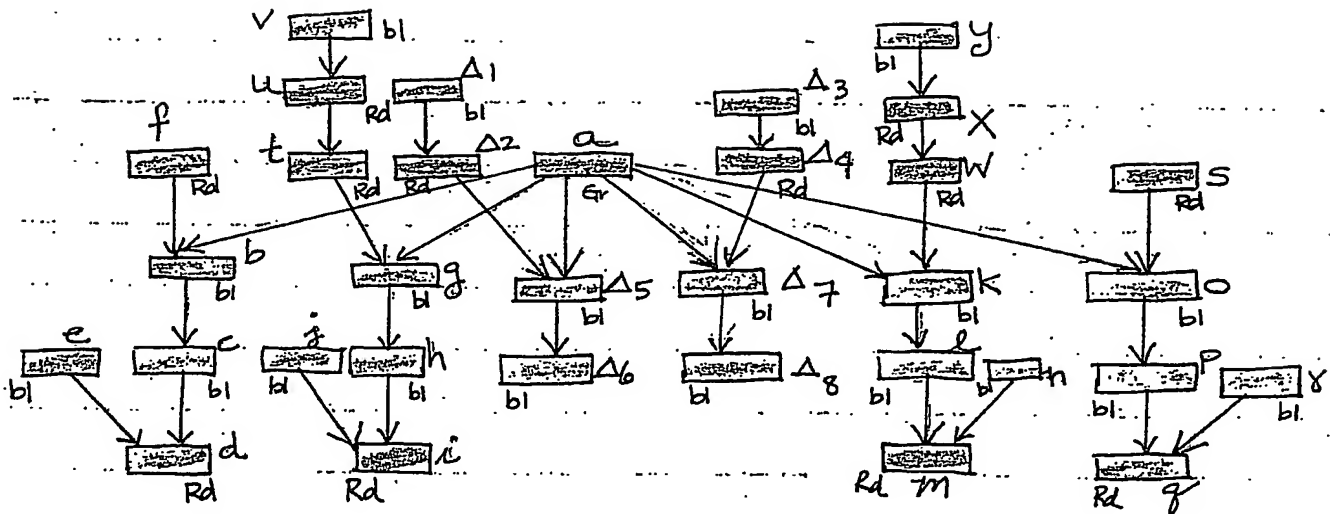
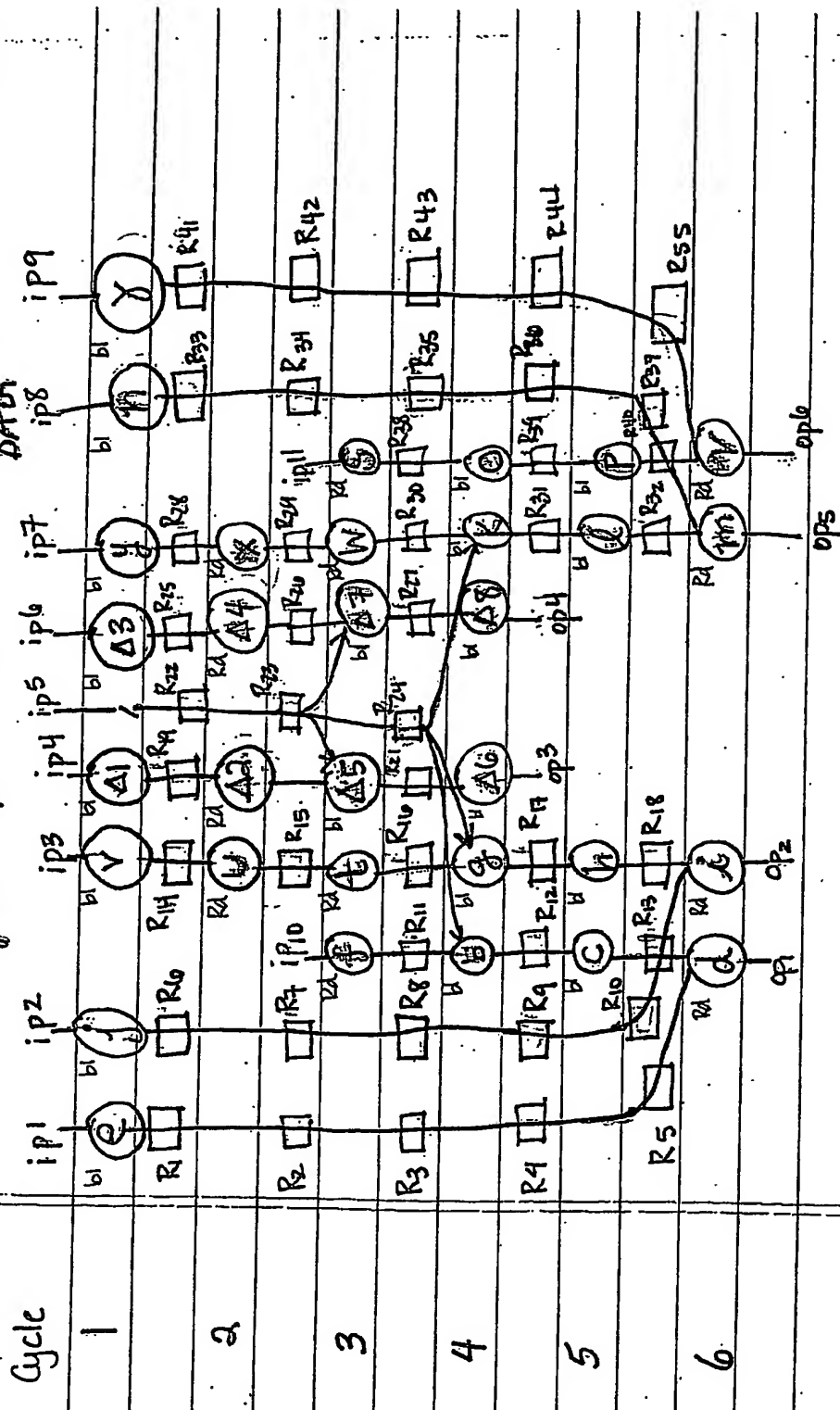


Fig. 5

KEY:  
 Rd = +, -  
 Gr = ÷  
 bl = \*  
 pwp = memory transaction

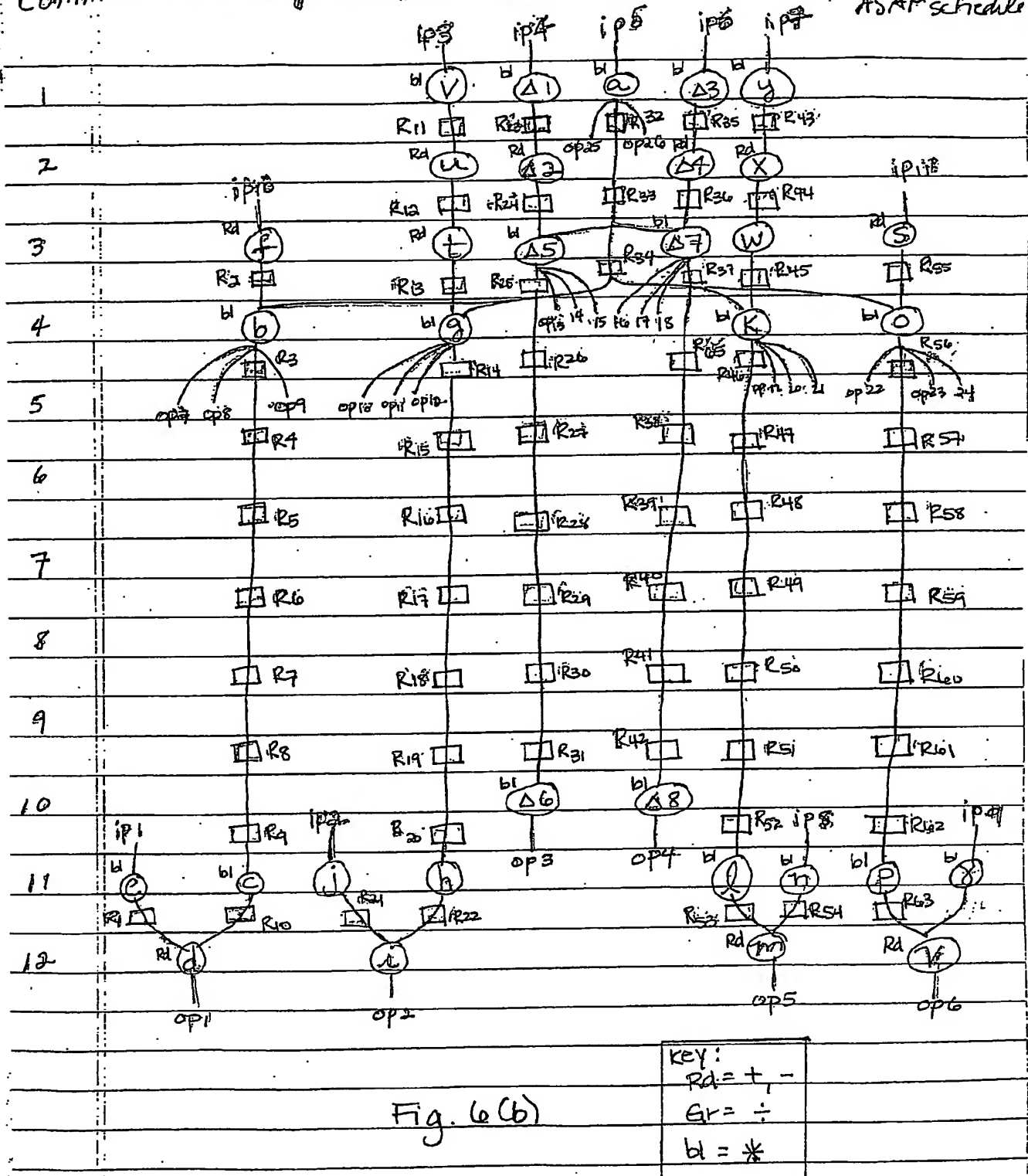
Common LC S-1 of Example mapped onto Affine with ASAP schedule



KEY:  
Rd = +  
Gr = ÷  
bl = \*

Fig. 6(a)

Common LCS-G of Example mapped onto Perspective DAG with ASAP schedule





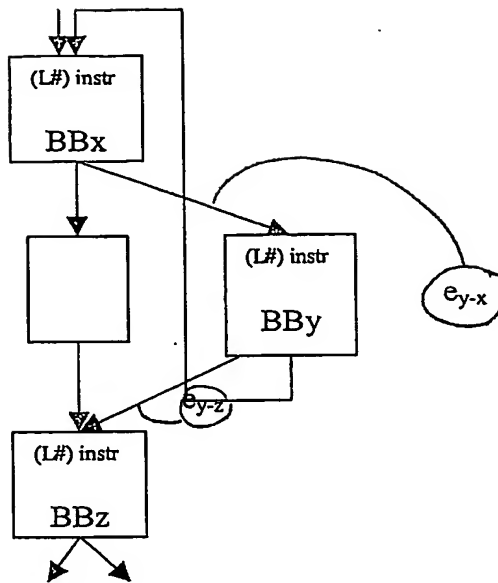


Fig. 7

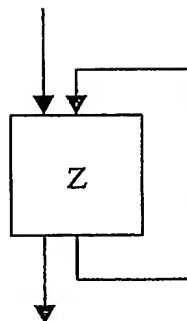


Fig. 8

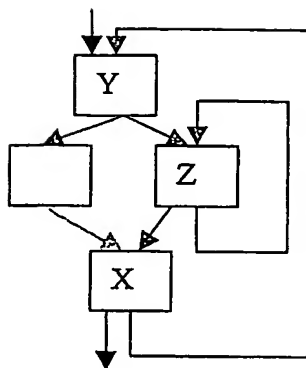


Fig. 9 (a)

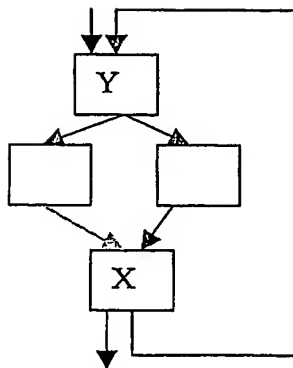


Fig. 9 (b)

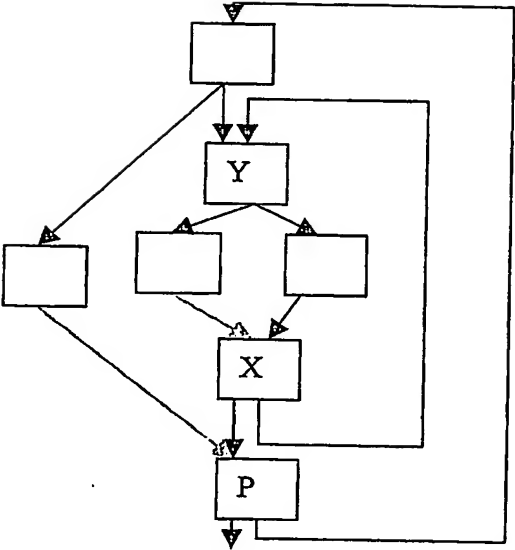
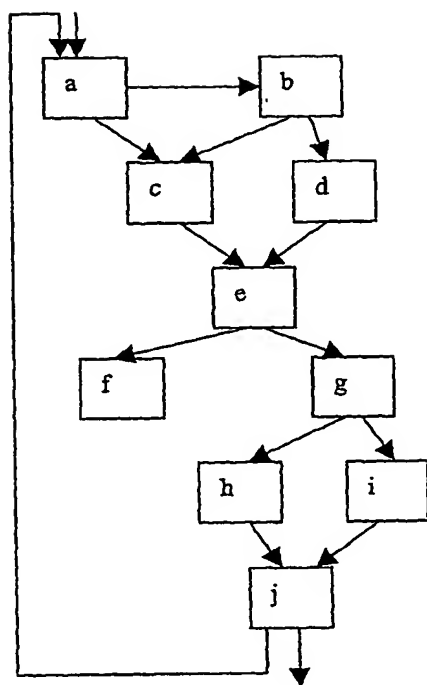


Fig. 10



Decision (a, b, e, g)

Merge (c, e, j)

Pass (d, f, h, i)

Fig. 11

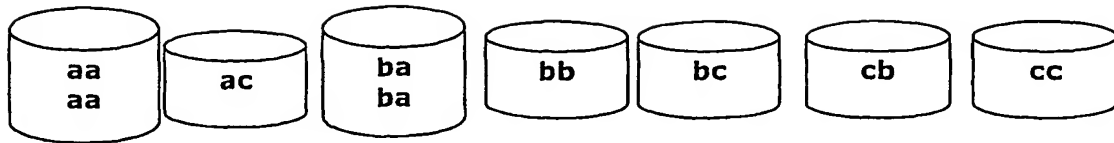
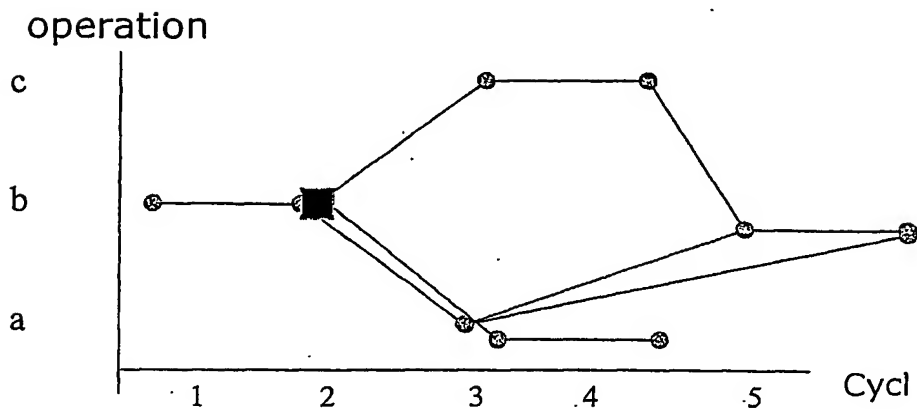


Figure 12: First Graph's edges arranged into a Bin Sequence



Graph number 2, Figure 13: The Second Graph

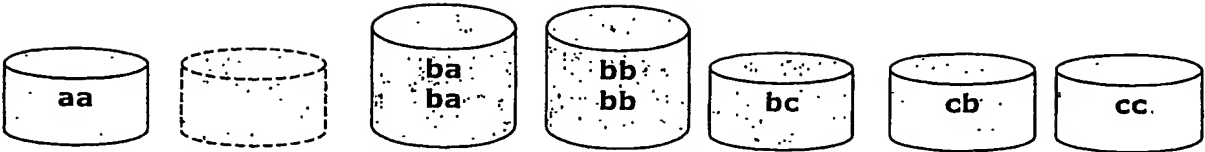


Figure 14. The Second Graph arranged in a Modified Bin Sequence

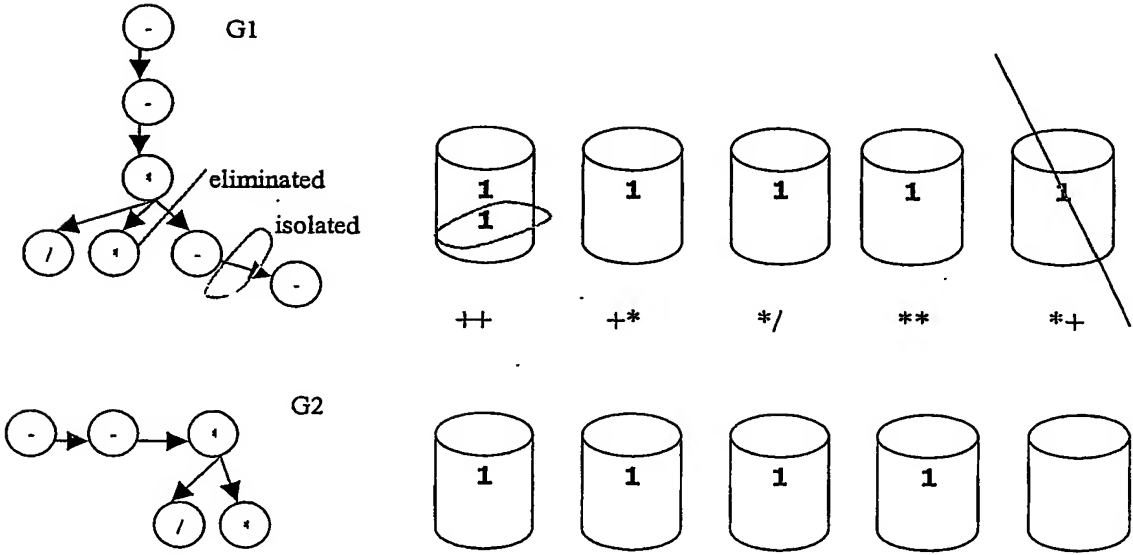


Fig. 14

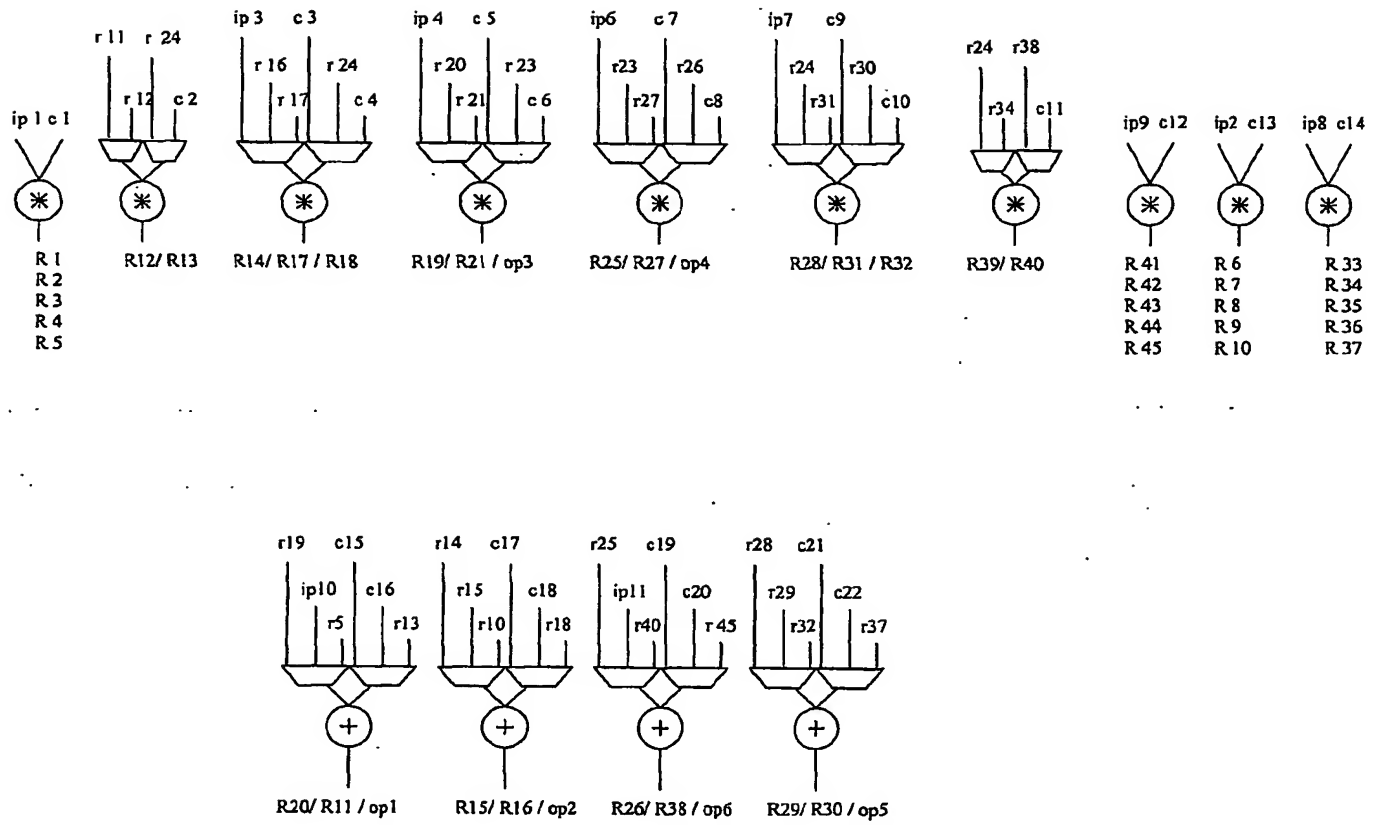


Fig. X Affine preloop common architecture after ASAP schedule

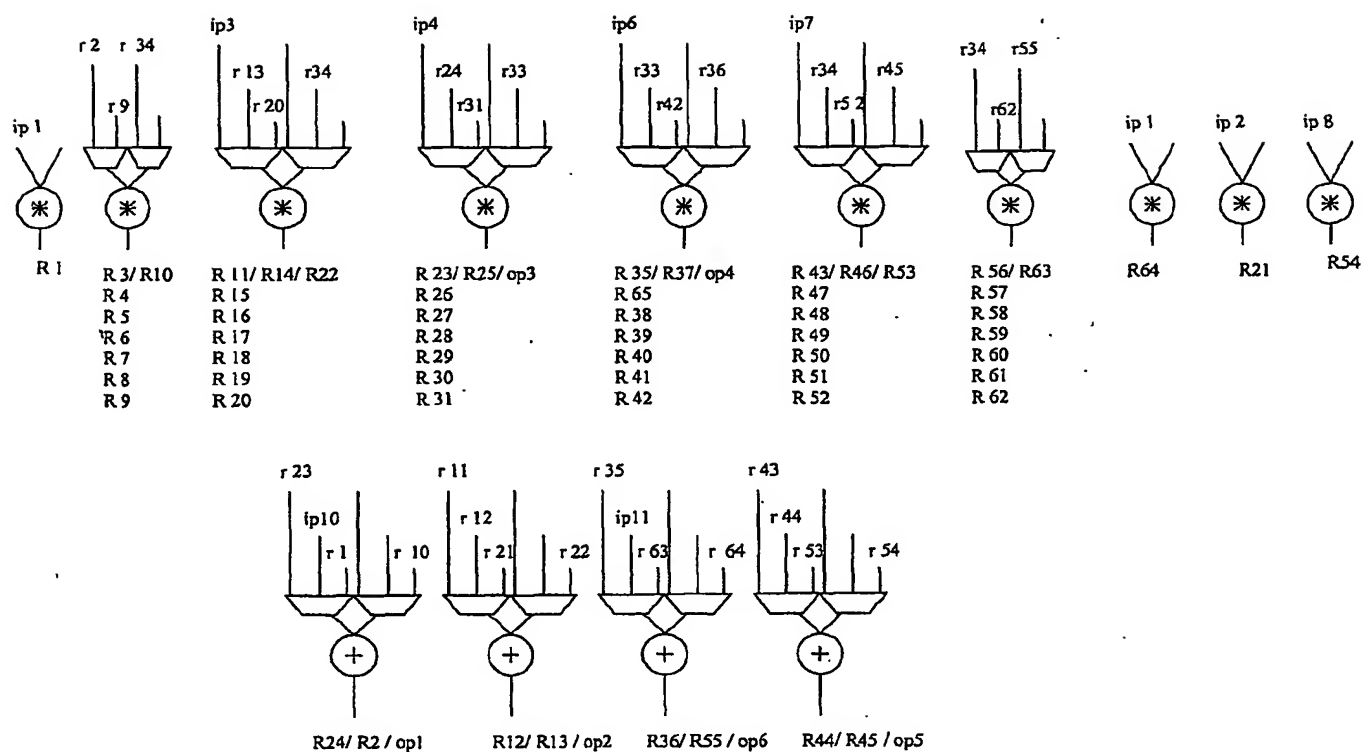
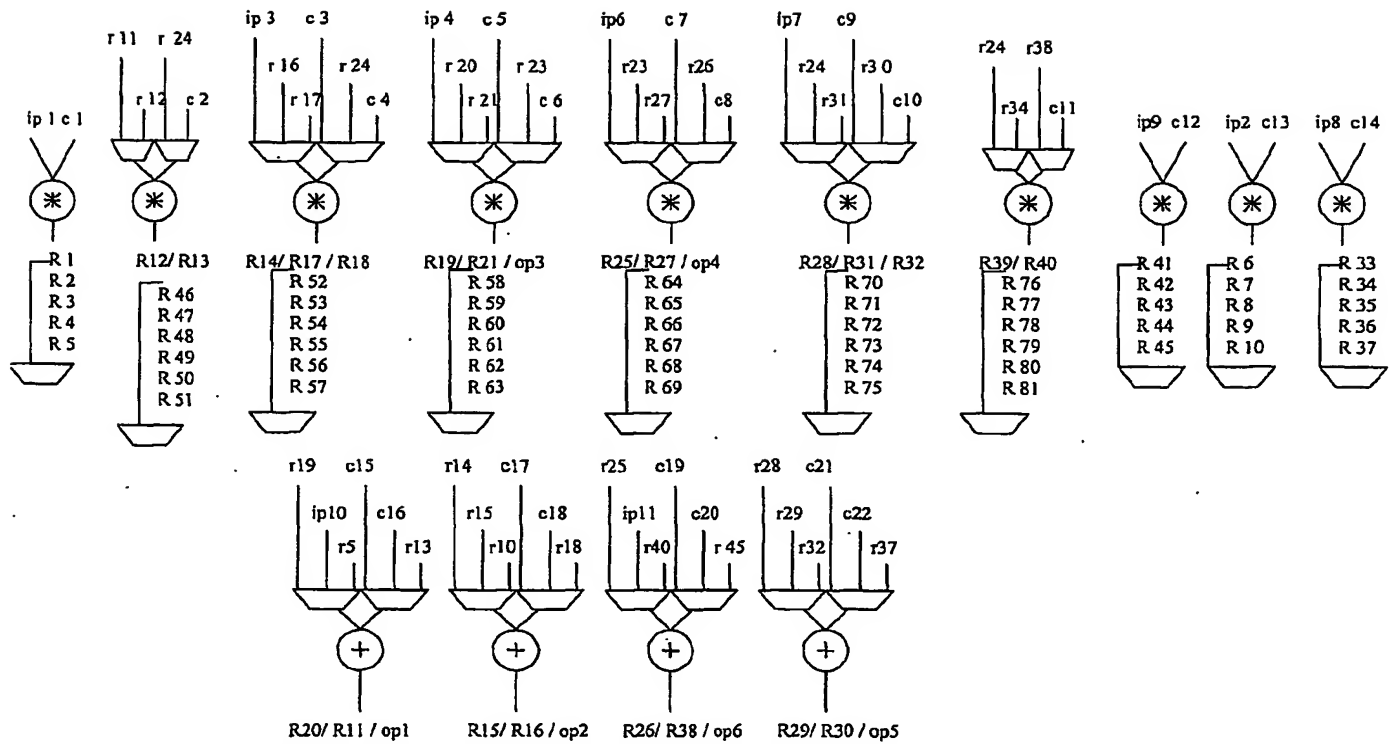


Figure 7: Perspective preloop common architecture after ASAP schedule





Note: Some multiplier and adder outputs also form outputs from the module.

Figure 2 Common architecture with multiplexers in delay paths to accommodate both affine and perspective instantiations.

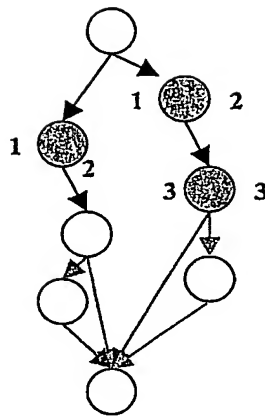
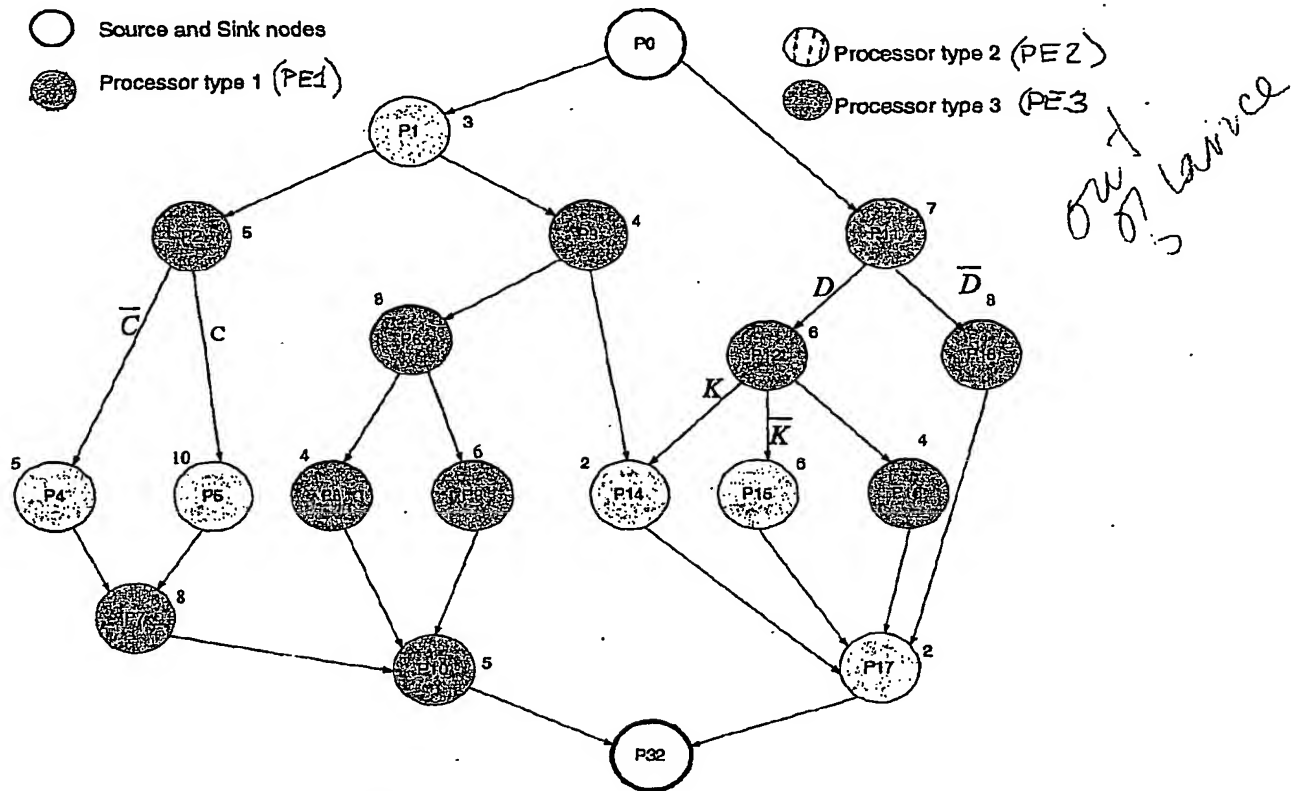


Figure 12: Path based edge activation

## ~~Illustrative example for our scheduling algorithm~~

*A* This example demonstrates <sup>the</sup> our initialization strategy. It describes how the CDFG is split into individual DFGs. Moreover, it also shows the various fields required for each node and edge.

### ~~A. Initial CDFG:~~



For the CDFG of Fig. 13x

**B. Initialization of CDFG data structure and Branching tree** proceeds as follows:

Var\_indices: var[0] = D; var[1] = C; var[2] = K;

Assume number of processing elements of type = 1

Branching tree paths: DCK, DCK', DC'K, DC'K', D'CK, D'CK', D'C'K, D'C'K'

Branching tree paths not possible: D'CK, D'CK', D'C'K, D'C'K'

Removing K we get: D'C, D'C'

Final Branching tree paths: DCK, DCK', DC'K, DC'K', D'C, D'C'.

Table xx and yy are the node and edge lists, respectively, for the CDFG of Fig. 13x. Figs. 14x-19x are the individual Data Flow Graphs (DFGs) of the CDFG of Fig. 13x.

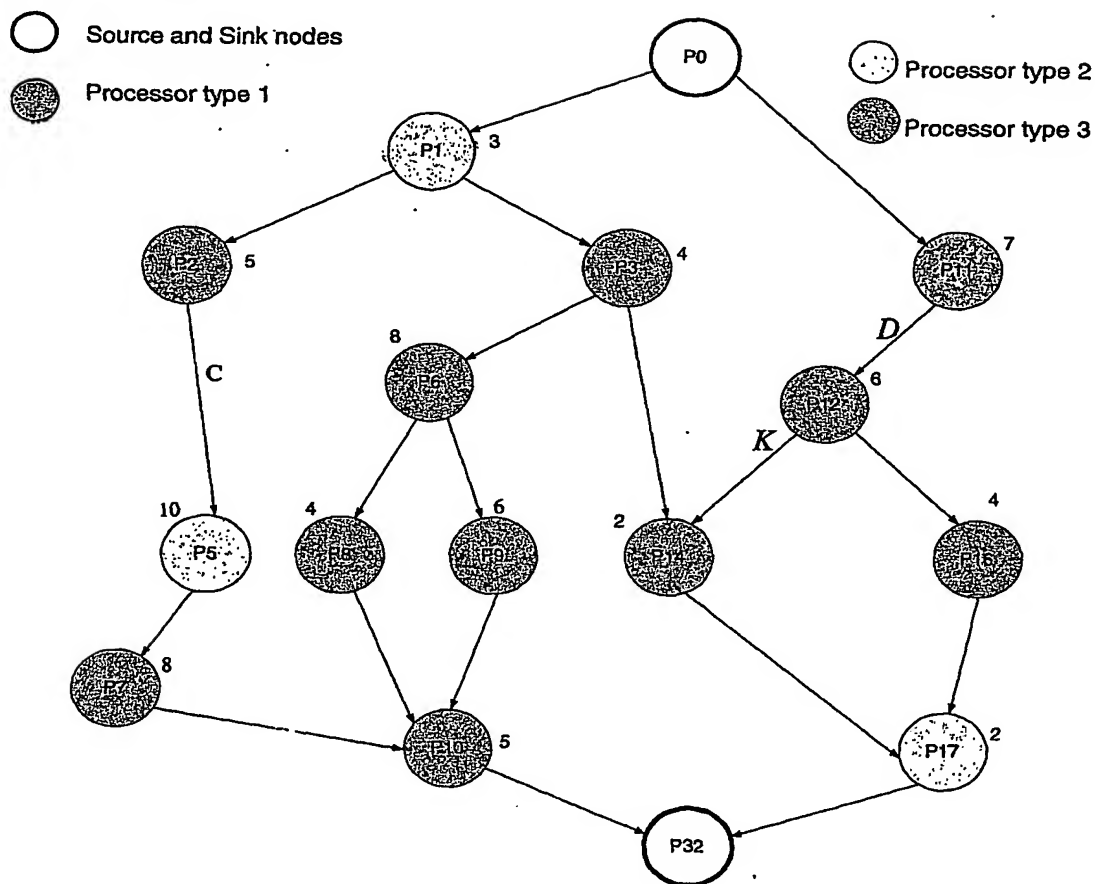
**C. List of individual DFGs:**DFG[0]  $\rightarrow$  DCK

Fig 14x

DFG[1]  $\rightarrow$  DCK'

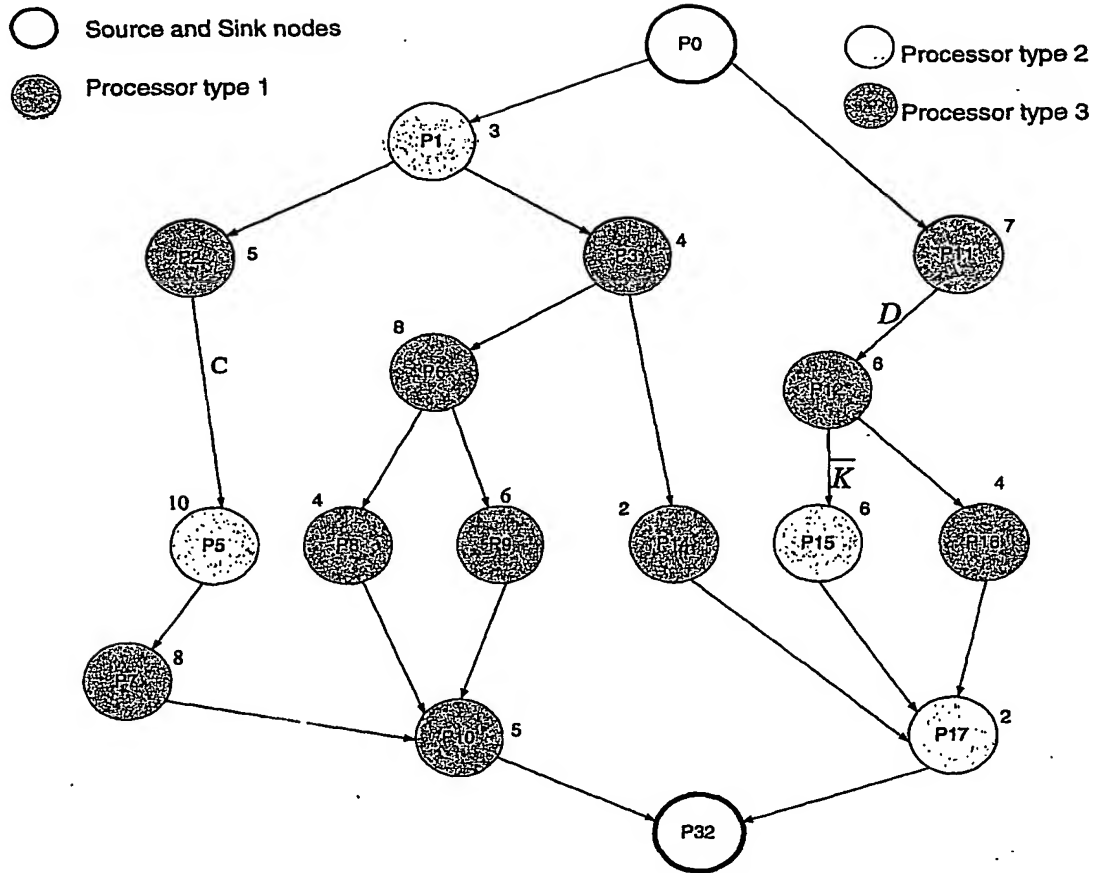


Fig. 15x

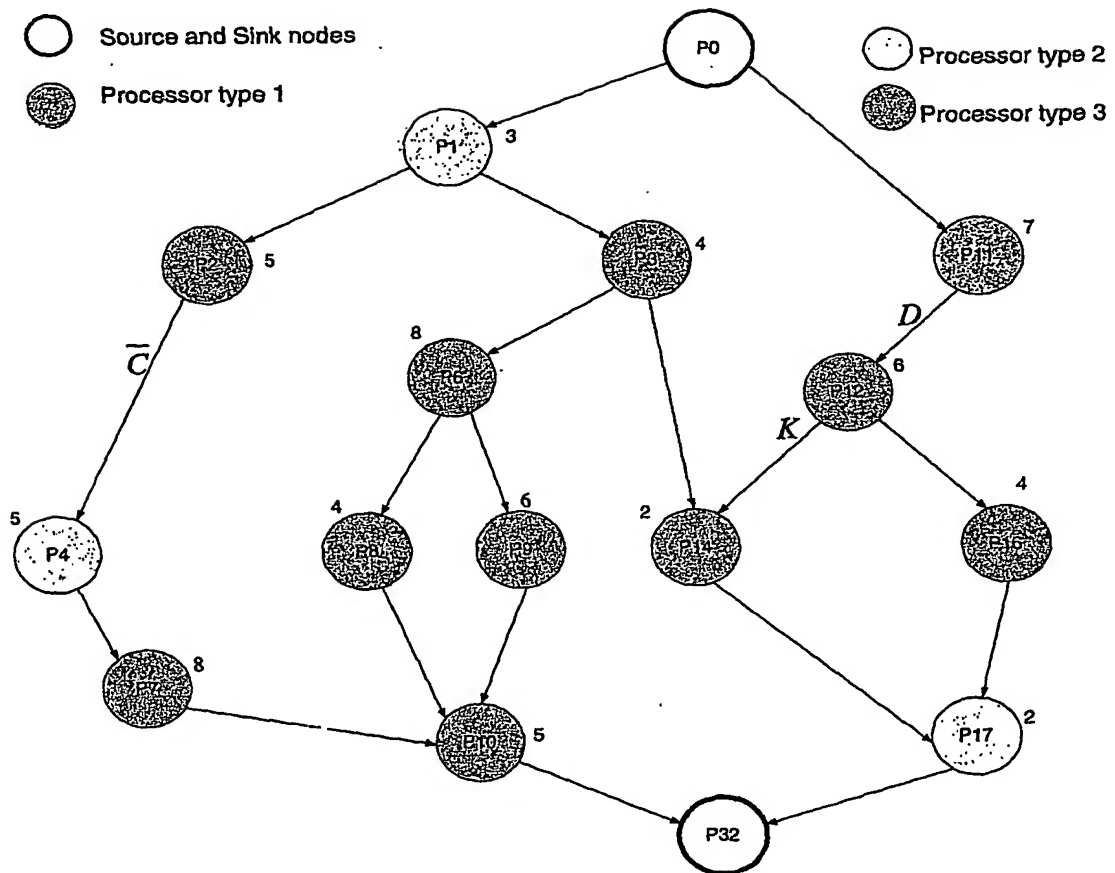
DFG[2]  $\rightarrow$  DC'K

Fig. 16X

DFG[4]  $\rightarrow$  D'C

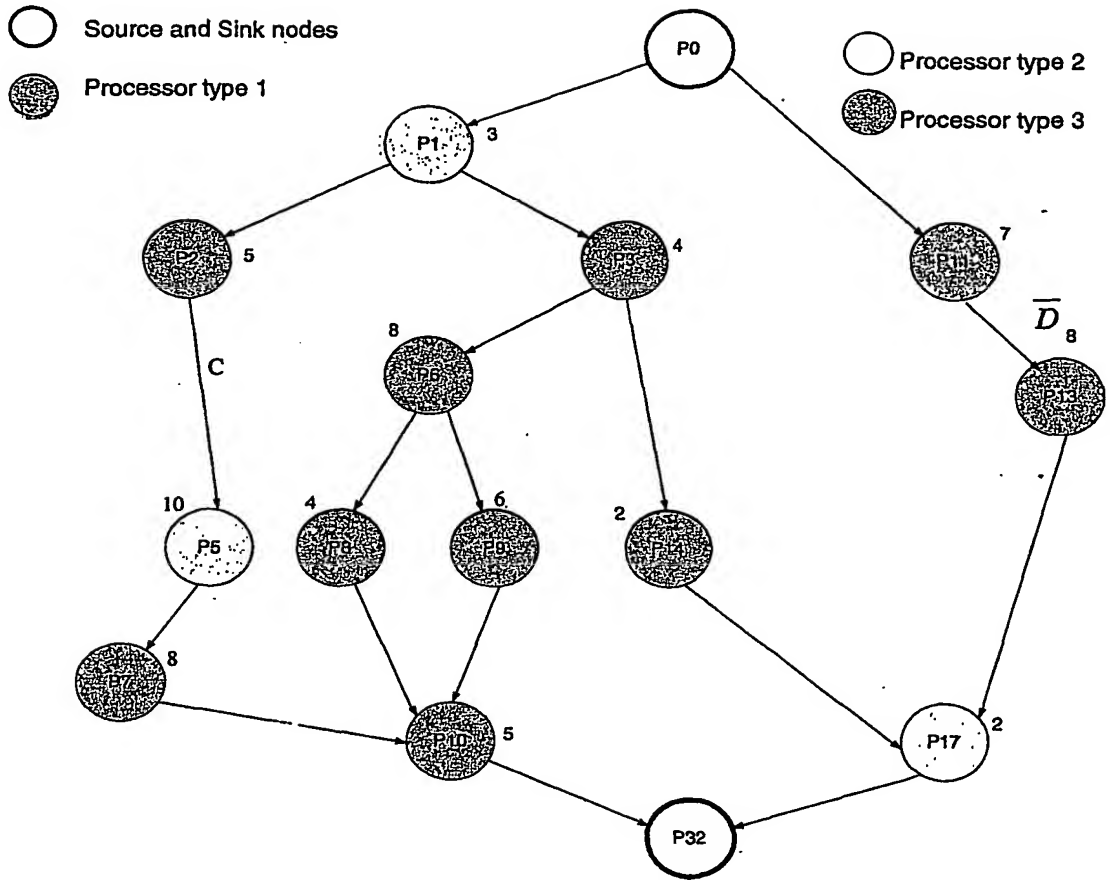
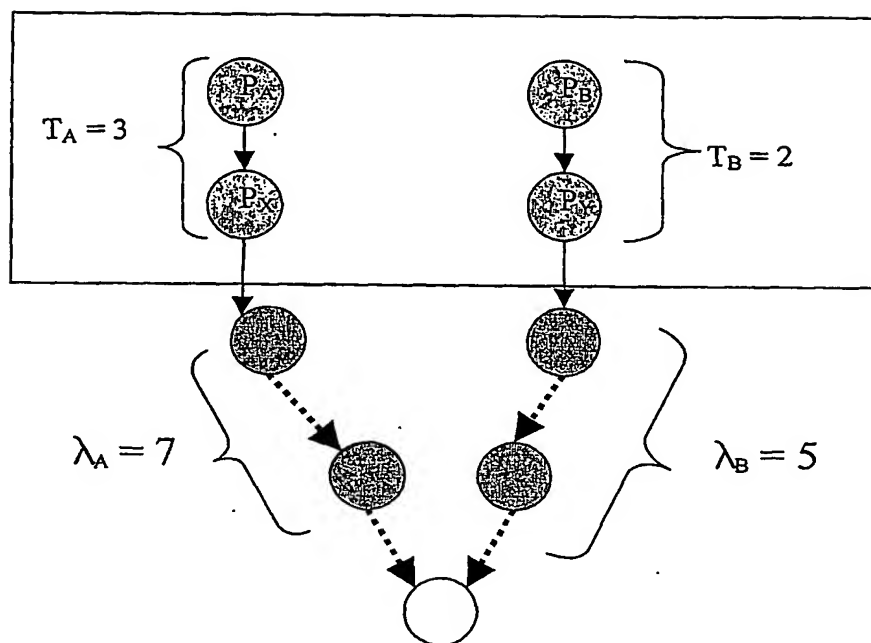


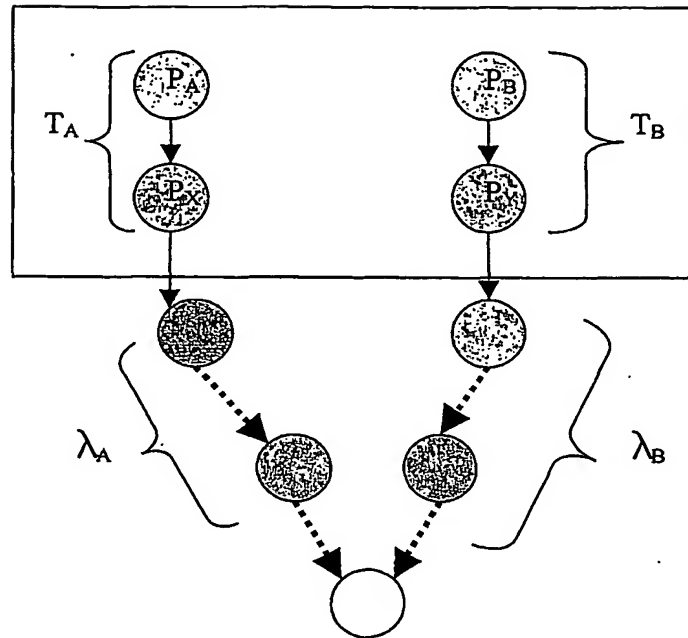
Fig 18x



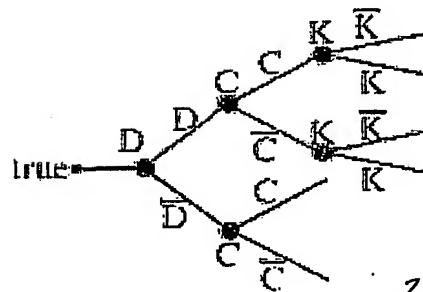




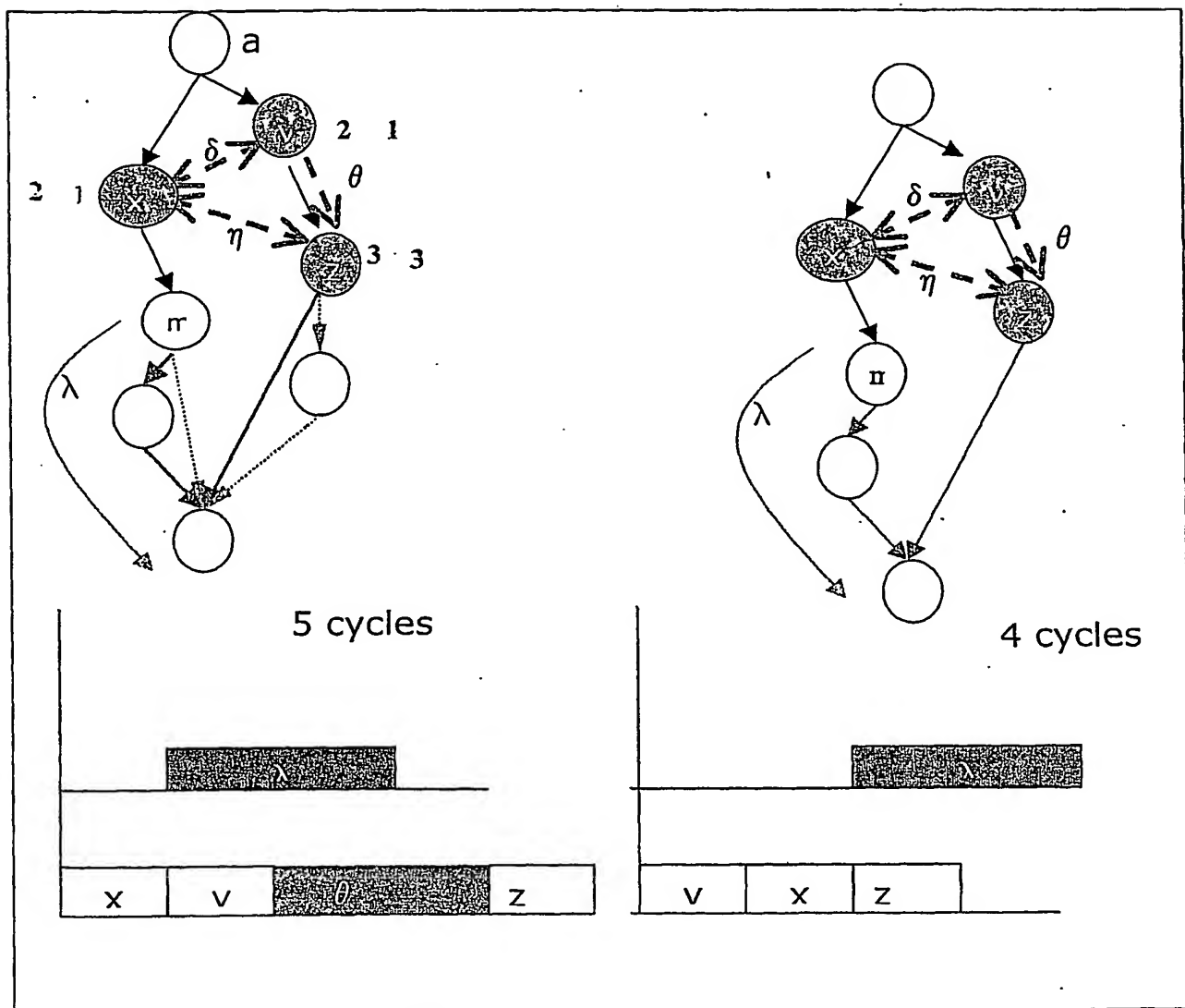
20X  
Figure 15: PCP Scheduling with Resource Dependencies in the Partial Path Region



21x  
Figure 14: PCP based Scheduling



22x  
Figure 16: Branching Tree



235  
Figure 17: Influence of Reconfiguration time on Scheduling

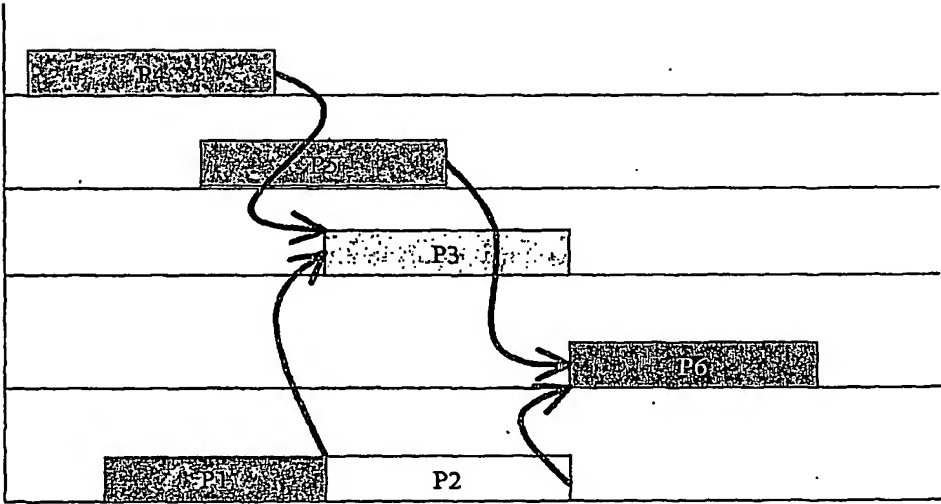


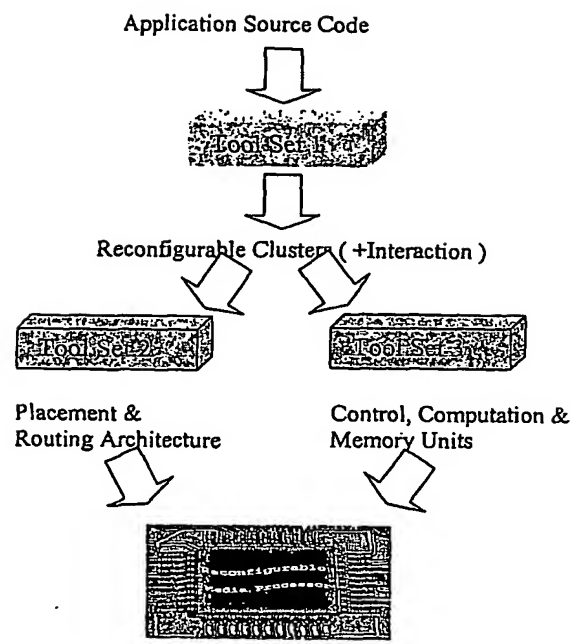
Figure 18: Scheduled Process Charts with Resource and Data Dependency  
24X

	Expression $\alpha$	Expression $\beta$	Expression $\theta$	Expression $\gamma$
Process A		0		
Process B		10		
....				
.....				

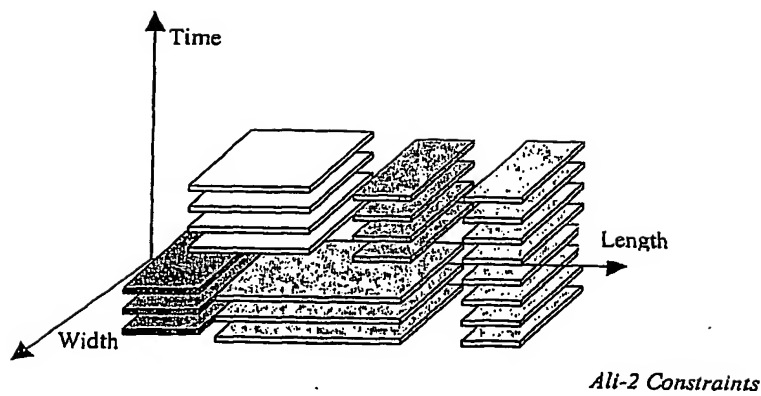
	Expression $\alpha$	Expression $\beta$	Expression $\theta$	Expression $\gamma$
Process A		30		
Process B		40		
....				
.....				

.....  
 ↓ and so on.

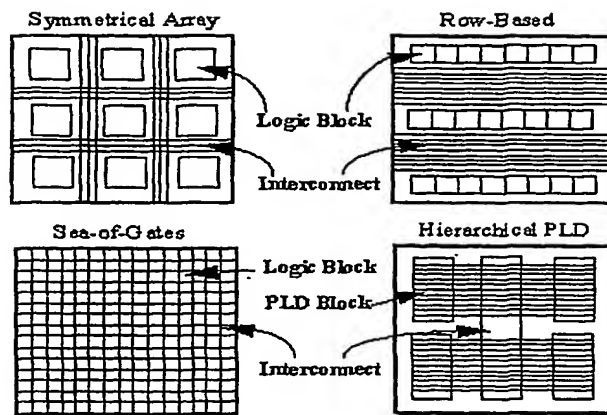
25X  
 Figure 19: Dynamic Entry Updates in the NSM and LSMs



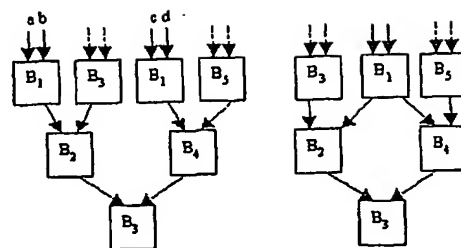
Ali-1 Tool Set Overview



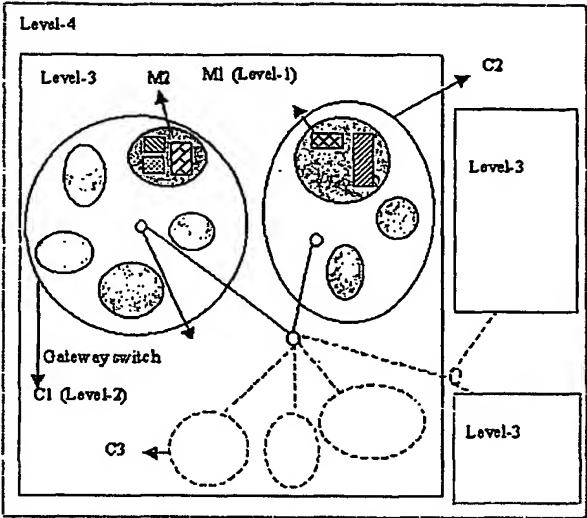
Ali-2 Constraints



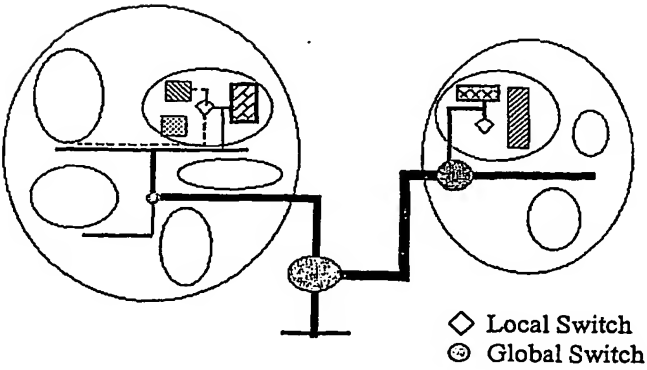
Ali-3 Routing Architecture Overview



(a) Multiple Building Block  
 (b) Single Building Block  
 Ali-4 Multiple vs. Single Building Block

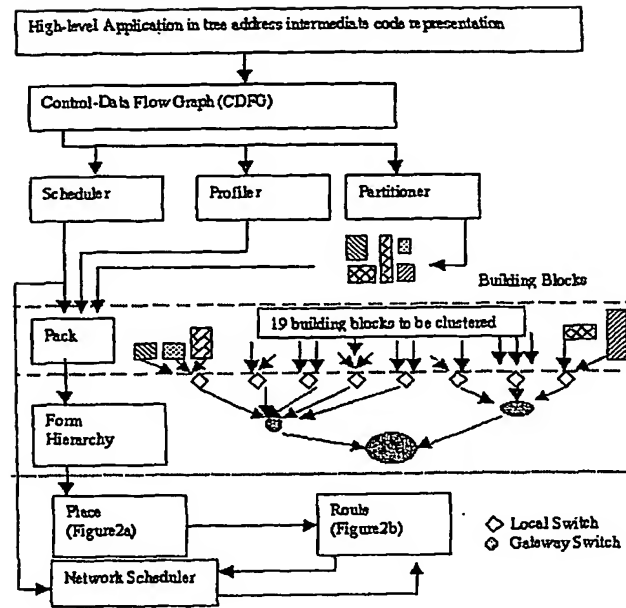


Ali-5 Overall Architecture

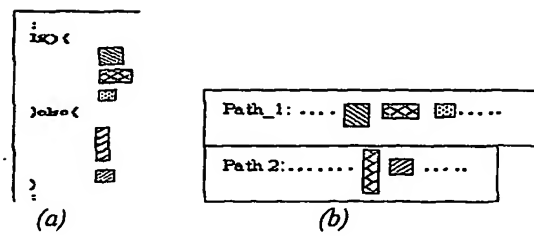


Ali-6 Switching



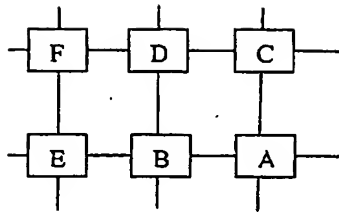
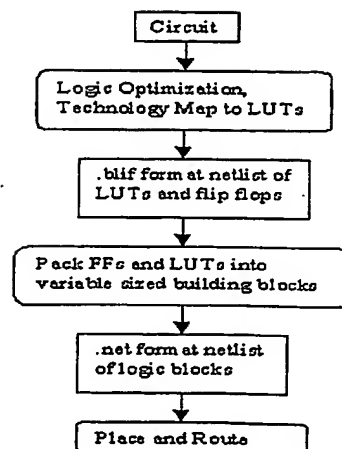


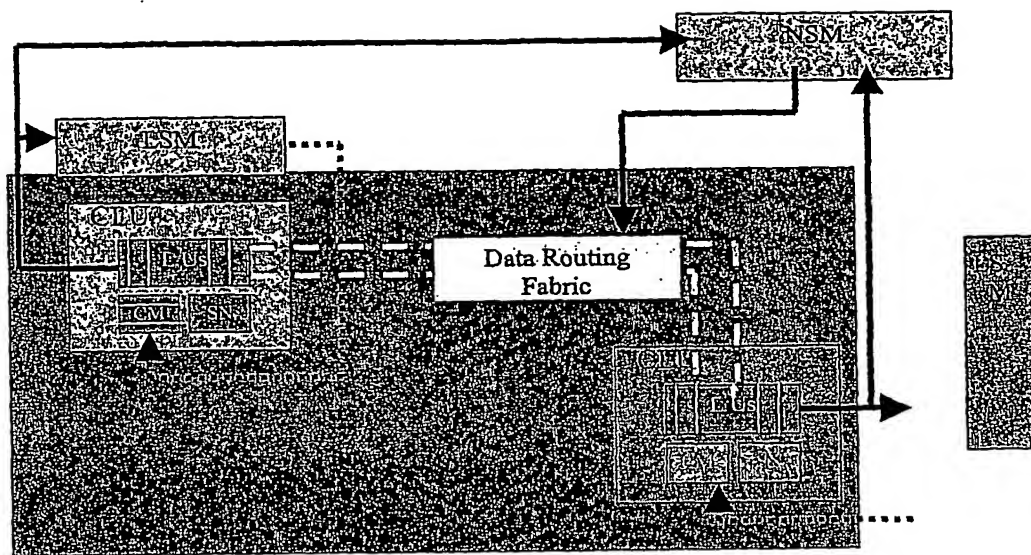
Ali-7 Methodology



Ali-8 Control Flow Effect on Clusters

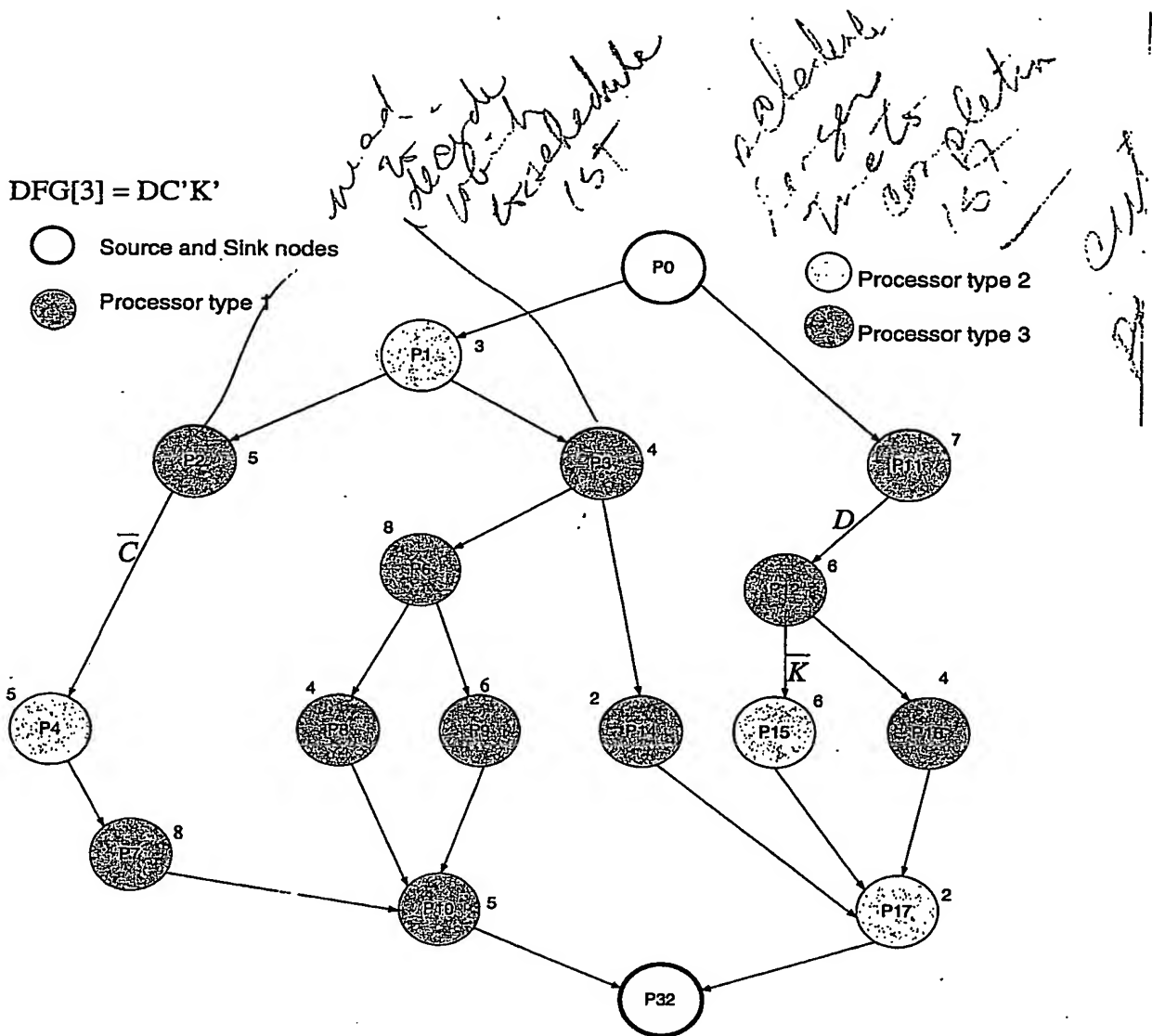
	A	B	C	D	E	F
A	0	X	X	X	X	X
B	5	0	X	X	X	X
C	6	0	0	X	X	X
D	4	3	7	0	X	X
E	1	4	1	0	0	X
F	3	0	4	5	3	0

*Ali-9a Cost matrix**Ali-9b Pre-placement**Ali-10 Design Flow*



CLU = Configurable Logic Unit; LU = Logic Units; SN = Switching Network  
 CM = Configuration Memory; LSM = Logic Schedule Manager

Figure 21: The Internals of the Reconfigurable Unit



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